Zero Inductor Voltage Multilevel Bus Converter

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***Abstract*—A novel topology to achieve 4:1 voltage step down, aimed at 48 volt to 12 volt conversion, is presented. The primary application for 48 volt to 12 volt conversion is for server power supplies as part of an Intermediate Bus Architecture, as Google and other large companies are pushing to switch from 12 volt to 48 volt server architecture to improve the performance of their data centers. The topology presented in this paper makes use of multi-level switching with flying capacitors to minimize the voltage stress of the switches, allow for significant reduction in the size of the magnetic components by reducing the voltage applied to the inductor, and enable low switching frequencies to be used. The switching scheme used in the topology causes the output inductor to see only the capacitor ripple voltage across its terminals. As this inductor sees almost zero voltage, the ripple current and reliance on magnetics is significantly reduced in this circuit. Through these advantages, the topology can achieve a peak efficiency of 99.5% for 48 volt to 12 volt conversion.**

Keywords— DC-DC converter; datacenter; intermediate bus

I. INTRODUCTION

As consumer demand for data and internet services grows, so too grows the strain placed on the servers and datacenters that handle this demand. In 2013 datacenters in the United States consumed 91 billion kilowatt-hours of electricity, and as the number of datacenters worldwide continues to increase exponentially this power consumption is expected to reach 190 billion kilowatt-hours in 2020. This has led to Google proposing and implementing 48 volt server architecture to replace the ubiquitous 12 volt architecture in use by most companies today. Figure 1 outlines the "2-Stage Conversion Approach" proposed by Google [1].

In order to maximize efficiency, DC distribution systems are widely used in datacenters [2]. One particularly attractive solution to maximize the benefits of the DC distribution is the use of the Intermediate Bus Architecture, as illustrated in Figure 1. The advantages of the Intermediate Bus Architecture include a reduction in the "upstream" AC-DC conversion losses, as well as a significant reduction in the DC bus distribution losses by enabling the use of a higher voltage DC bus. In this architecture a DC-DC converter called the Intermediate Bus Converter (IBC) steps down the DC bus voltage, nominally around 48 volts, to a lower level that can be more easily and efficiently converted by the point-of-load (POL) converters. Typically the step down ratio provided by the IBC will be between 4:1 and 6:1. In the Intermediate Bus Architecture the IBC can provide an unregulated output voltage, as the POL converters can provide load regulation to the low-voltage electronic devices. Optimization and improvements to the technology used in the IBC is a critical and active area of research for improving the efficiency of the Intermediate Bus Architecture [3] [4].

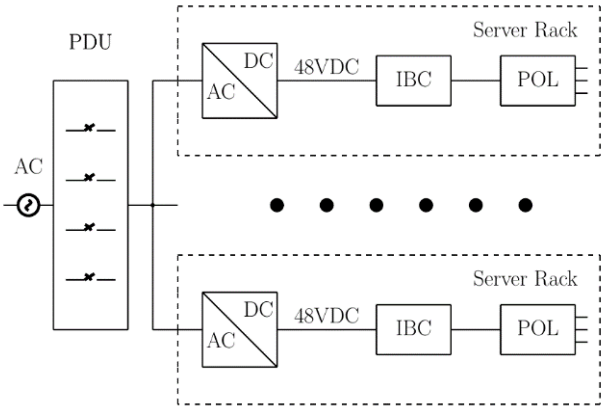

Fig. 1. Google's 48V Server Architecture "2-Stage Conversion Approach"

The motivation of this paper is to present a novel IBC topology that achieves 4:1 voltage step down, particularly aimed at 48 volt to 12 volt conversion. Two existing technologies used to achieve this 48 volt to 12 volt conversion are examined. The first is the switched-capacitor voltage divider, and shown in Figure 2. The key drawback of this topology is that, during the operation the capacitors will be connected in parallel through the MOSFET's at the time of switching. Thus, due to the capacitor ripple voltage, the MOSFET's will carry high peak current during switching, lowering the efficiency and necessitating higher switching frequencies be used.

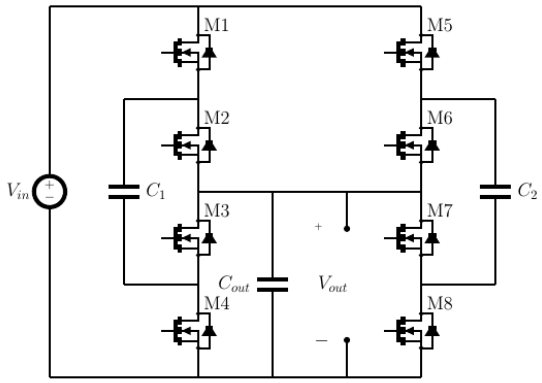

Fig. 2. Switched Capacitor Voltage Divider Circuit

A second method is using a switched capacitor converter with an inductor added to form a resonant circuit [5][6]. This will reduce the peak current through the MOSFET's during switching, but the performance becomes highly sensitive to the inductor tolerance which can compromise the design. Additionally the inductor, particularly the core loss, will typically be a significant source of loss in this topology. The solution presented in this paper is a novel topology to convert a 48 volt DC input to a 12 volt DC output with extremely high efficiency of up to 99.5% while allowing the use of inductors as small as 100nH. The ability to meet or exceed the performance of a resonant circuit, without requiring a complex design that is sensitive to component tolerances is a key advantage of the proposed topology. The inductor loss is also minimized through the zero inductor voltage operation concept presented in the paper.

48 volt to POL is sometimes proposed as an alternative to the Intermediate Bus Architecture, wherein one converter is used to directly convert the 48 volt bus to the point of load voltage, which is typically very low, around 1 volt, for server applications. Using current technology, it is very difficult to convert 48 volts to 1 volt at high efficiency, and the efficiency is significantly lower than for 12 volt to 1 volt conversion, as outlined in Google's "Direct Conversion Approach" [1]. Thus, an intermediate bus converter capable of achieving extremely high efficiency (>98%) will enable the Intermediate Bus Architecture to remain a superior option.

The organization of the paper is as follows. Section II will explain the operation of the circuit, and highlight the key advantages of the topology; namely the zero inductor voltage concept, and the voltage stress reduction offered by the flying capacitors. Simulation results will also be presented in this section to validate the analysis. Section III will provide an analysis of the power loss of the topology. Section IV provides experimental results to verify the performance of the topology, and Section V will conclude the paper.

II. Operating Principles and Analysis

A. Circuit Topology and Operation

The circuit diagram of the proposed topology is presented in Figure 3.

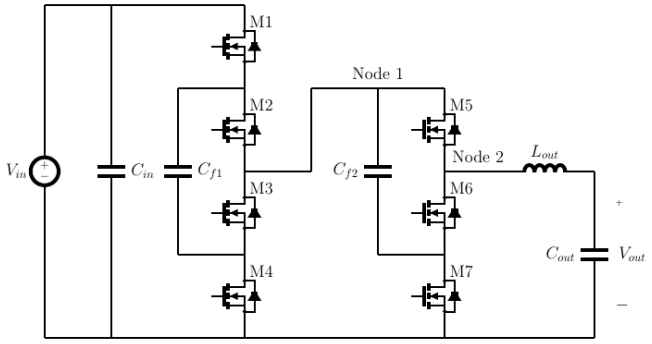

Fig. 3. Circuit Diagram of the Proposed Topology

This topology uses seven MOSFET's, two flying capacitors, an output LC filter, and an input capacitor to achieve an unregulated 4:1 voltage step down. The gate signal diagram for the MOSFET's is presented in Figure 4.

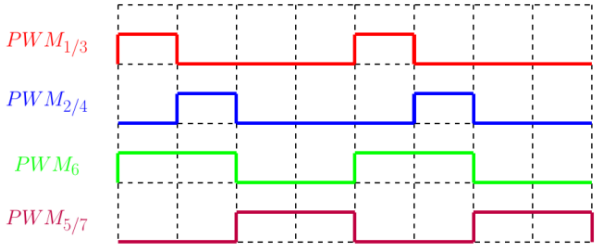

Fig. 4. PWM Gate Signal Diagram for the Proposed Circuit

The MOSFET's are driven pair-wise with fixed duty cycle. The operation of the circuit can be understood by examining the three states created by the gate signals. Under steady state operation, the first flying capacitor is nominally charged to half of the input voltage, and the second flying capacitor is charged to one quarter of the input voltage. The output voltage of the converter can be evaluated by examining the inductor voltage balance; for one complete cycle the average inductor voltage must equal zero.

In State A, pictured in Figure 5, MOSFET's M1, M3 and M6 are turned on. Both flying capacitors are charged by the input source.

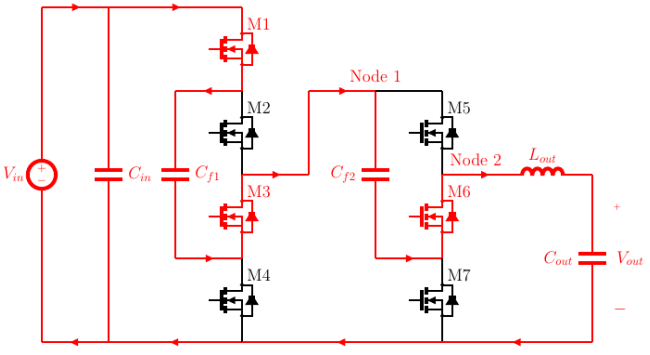

Fig. 5. Circuit State A: Active Components Highlighted in Red

In State A the inductor voltage can be expressed as:

$$V_{LA} = V_{in} - V_{cf1-A} - V_{cf2-A} - V_{out} \quad (1)$$

In State B, shown in Figure 6, MOSFET's M2, M4 and M6 are turned on. In this state the first flying capacitor is now discharging, while the second flying capacitor continues to charge.

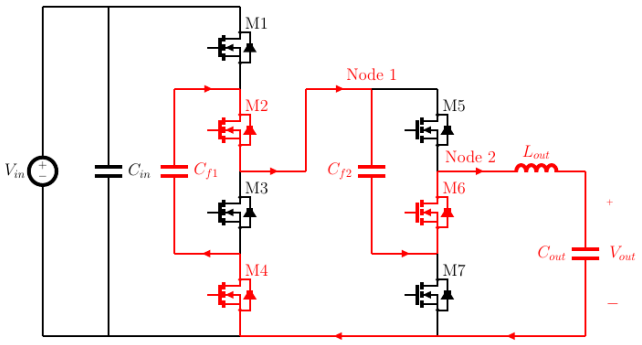

Fig. 6. Circuit State B: Active Components Highlighted in Red

$$V_{LB} = V_{cf1-B} - V_{cf2-B} - V_{out} \quad (2)$$

In State C, illustrated in Figure 7, MOSFET's M5 and M7 are turned on. In this state the first flying capacitor is no longer connected and the second flying capacitor is now discharging.

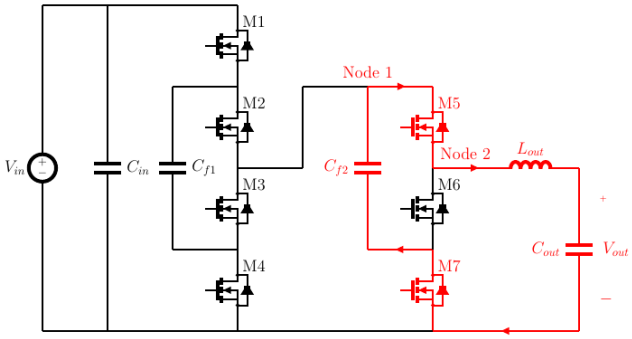

Fig. 7. Circuit State C: Active Components Highlighted in Red

$$V_{LC} = V_{cf2-C} - V_{out} \quad (3)$$

As seen from the gate signal diagram, State A is active for 25% of one cycle, State B is active for 25% of one cycle, and State C is active for the remaining 50% of the cycle. Thus the average inductor voltage can be expressed as:

$$V_L = \frac{V_{LA}}{4} + \frac{V_{LB}}{4} + \frac{V_{LC}}{2} \quad (4)$$

$$V_L = \frac{V_{in}}{4} - \left(\frac{V_{cf1-A}}{4} + \frac{V_{cf1-B}}{4}\right) - \left(\frac{V_{cf2-A}}{4} - \frac{V_{cf2-B}}{4} + \frac{V_{cf2-C}}{2}\right) - (V_{out}) \quad (5)$$

Note that the capacitor balance must also be maintained for steady state operation. This means that the average voltage of C_{f1} for State A must be equal to the average voltage of C_{f1} for State B, and the average of C_{f2} across both State A and State B must be equal to the average voltage of C_{f2} across state C. Thus we can simplify the equation by noting the following:

$$V_{cf1-A} = V_{cf2-B} \quad (6)$$

$$\frac{V_{cf2-A} + V_{cf2-B}}{2} = V_{cf2-C} \quad (7)$$

Under steady state operation the inductor voltage must equal zero, and as all the capacitor voltage terms cancel out with the above substitutions we are left with:

$$V_{out} = \frac{Vin}{4} \quad (8)$$

Thus, the converter achieves 4:1 voltage step down. By examining the equivalent circuits for States A through C we can see that a significant problem with the switched capacitor converter is not an issue for this topology; namely the paralleling of capacitors during switching.

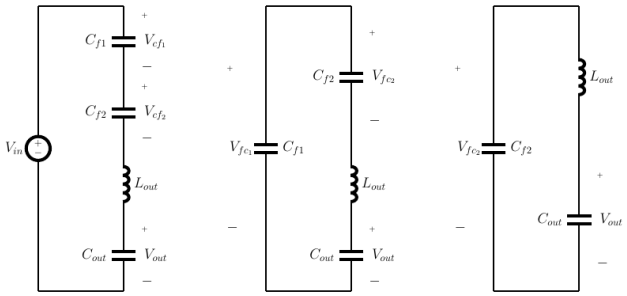

Fig. 8. Equivalent Circuits of Each Operating State

During all switching states the capacitors are charged and discharged through the output inductor, and never connected in parallel. Thus the issue of high peak current during switching is avoided in this circuit.

B. Detailed Inductor Voltage Analysis

A key advantage of this topology, namely the zero inductor voltage operation, can be seen by examining the voltage at Node 2. Recall that the first flying capacitor is charged to 1/2 of the input voltage nominally, and the second flying capacitor is charged to 1/4 of the input voltage nominally. These capacitor voltages can be expressed as a nominal DC value, summed with a ripple voltage.

For State A:

$$v_{n2} = V_{in} - v_{cf1} - v_{cf2} \quad (9)$$

$$v_{n2} = V_{in} - \frac{V_{in}}{2} - \frac{V_{in}}{4} - v_{cf1rip} - v_{cf2rip} \quad (10)$$

$$v_{n2} = \frac{V_{in}}{4} - v_{cf1rip} - v_{cf2rip} \quad (11)$$

For State B:

$$v_{n2} = v_{cf1} - v_{cf2} \quad (12)$$

$$v_{n2} = \frac{Vin}{2} - \frac{Vin}{4} + v_{cf1rip} - v_{cf2rip} \quad (13)$$

$$v_{n2} = \frac{V_{in}}{4} + v_{cf1rip} - v_{cf2rip} \quad (14)$$

For State C:

$$v_{n2} = v_{cf2} \quad (15)$$

$$v_{n2} = \frac{V_{in}}{4} + v_{cf2rip} \quad (16)$$

For all of the above states, the voltage at Node 2 is equal to $1/4V_{in}$ summed with a voltage due to the capacitor ripple. The inductor is connected between Node 2 and the output voltage, which was shown to equal $1/4V_{in}$. Then the inductor voltage is given by:

$$v_L = \frac{V_{in}}{4} - \frac{V_{in}}{4} + v_{ripple} = v_{ripple} \quad (17)$$

Thus, the inductor will see no DC voltage drop across its terminals. The inductor voltage is independent of the input and output voltages; the only voltage seen by the inductor will be due to the capacitor ripple. As a result of this the inductor loss in the circuit is minimized. The low voltage stress means that very small inductors, as small as 100nH, can be utilized even with switching frequencies below 100kHz.

C. *Practical Operating Considerations*

During practical operation, deadtime is required to be added to the PWM switching to prevent shoot-through. This results in the introduction of a fourth state, shown in Figure 9.

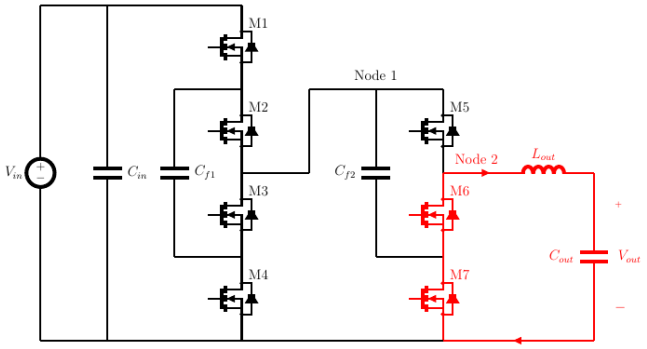

Fig. 9. Circuit State D: Active Components Highlighted in Red

During this time, the inductor current freewheels through the body diodes of M6 and/or M7. Note that during the transition between State A and State B M6 will remain on, thus only M7 will conduct through its body diode for this time. During the deadtime the voltage at Node 2 becomes equal to the diode drop of the reverse conducting MOSFET's. It is very important that this deadtime remain as short as possible for two reasons; the first being that the inductor current will drop quickly during the deadtime, and the second being that the conduction loss of the body diodes will be large, reducing the efficiency. In a well-designed circuit, this deadtime can be very short, on the order of tens of nanoseconds, allowing for very good performance to be achieved.

Additionally, the topology requires a soft-starting circuit to operate correctly. One key advantage offered by the flying capacitors is that they reduce the voltage stress of each MOSFET to $1/2V_{in}$ for M1-M4, and to $1/4V_{in}$ for M5-M7. Thus, lower voltage rating devices can be used to improve the performance, but, these devices will not be able to block the full input voltage. Thus, the flying capacitors must be pre-charged using a simple soft-starting circuit.

D. *Simulation Results*

Simulation was used to verify the operation of the proposed circuit topology. The simulation was conducted with the parameters listed in Table 1.

TABLE I. SIMULATION PARAMETERS

Simulation Parameters	Parameter Values
Input Voltage	48V
Load Current	25A
Frequency	60kHz
Deadtime	15nsec
Capacitor 1	100µF
Capacitor 2	200µF
Inductor	200µH

Figure 10 shows the converter input voltage, output voltage, the voltage of the two flying capacitors. From this figure it can be seen that the first flying capacitor maintains its voltage at $1/2V_{in}$, the second flying capacitor maintains its voltage at $1/4V_{in}$, and the output voltage is equal to $1/4V_{in}$.

Figure 11 shows the inductor voltage and the capacitor ripple voltage. Note that the capacitor ripple voltages are obtained by subtracting the nominal DC values of $1/2V_{in}$ and $1/4V_{in}$ respectively. The inductor voltage is shown to be equal to the sum of the capacitor ripple waveforms. Note that as the capacitors alternate between charging and discharging depending on the current state the inductor voltage is not a simple summation of these two waveforms, but rather the polarity of the capacitor voltage must be considered as shown in equations 9-16. The effect of the reverse conduction on the inductor voltage during the deadtime can also be seen in this Figure.

Figure 12 shows the currents of MOSFET's M1, M2 and M7 along with the flying capacitor voltage waveforms. This Figure demonstrates the reverse conducting state of M7 during the switching transitions.

The inductor current, as well as the current waveforms for the two flying capacitors is shown in Figure 13.

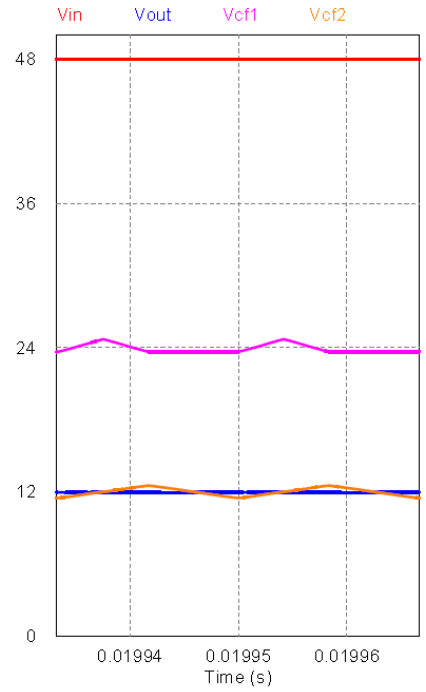

Fig. 10. Input, Output, and Flying Capacitor Voltage Waveforms

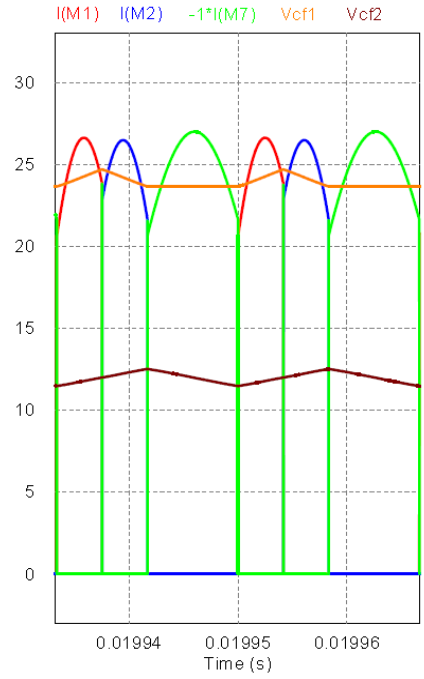

Fig. 12. MOSFET M1,M2 and M7 Currents and Capacitor Voltages

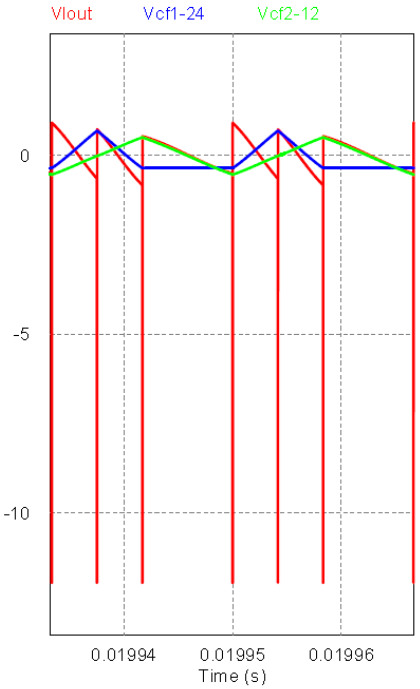

Fig. 11. Inductor and Capacitor Ripple Voltage Waveforms

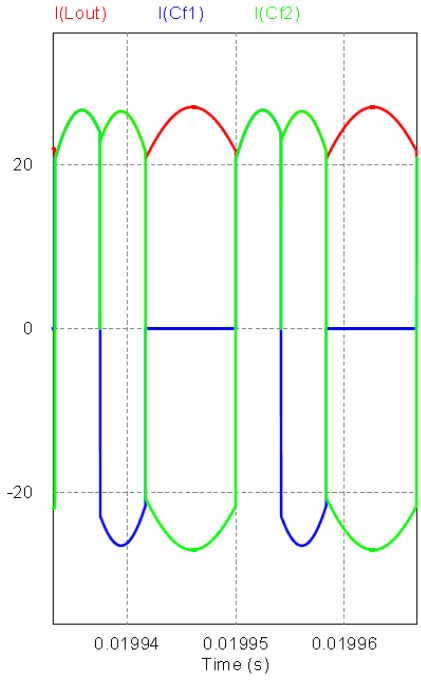

Fig. 13. Flying Capacitor and Inductor Current Waveforms

III. Operating Principles and Analysis

In order to optimize the design of the topology it is critical to understand the sources of loss within the circuit. While conducting, each MOSFET will carry the full output current. The first stage MOSFETs, M1-M4, are turned on with 25% duty cycle. The first stage flying capacitor will see 50% duty cycle, as will the second stage MOSFETs, M5-M7. The second flying capacitor and the inductor will see 100% duty cycle. As the RMS current seen by all of these devices will be dependent on the output current, it is important to minimize the resistance of each component to maintain high efficiency for high load currents. For the capacitors, ceramic capacitors are used, with multiple capacitors placed in parallel, to minimize the equivalent series resistance (ESR). For the MOSFETs, there is some level of trade-off between the switching losses, and the conduction losses. Despite being a hard-switching topology, the zero-inductor voltage concept and multilevel switching allows for very low switching frequency to be utilized, less than 100kHz. Thus, for this topology, the conduction loss is the dominant source of loss in the MOSFETs.

A power loss breakdown is presented in Figure 14. The components used in the analysis are presented in Table 2. The loss breakdown is presented for a load current of 25A and a switching frequency of 60kHz. This is selected to match with the experimental results presented in Section IV. As shown, the conduction loss is the dominant source of loss in the topology, making up 77% of the total loss in the circuit.

TABLE II. Loss Analysis Components

	Loss Analysis Components	
	Part Number	***Important Parameters***
M1-M4	BSC011N03LSI	R_{ds}=1.1mΩ Q_g=20nC
M5-M7	BSC009NE2LS5I	R_{ds}=0.95mΩ Q_g=17nC
Inductor	SLR1075-231	L=230nH DCR=0.29mΩ
Capacitor 1	10x10µF Ceramic	ESR=1.5mΩ
Capacitor 2	10x47uF Ceramic	ESR=0.75mΩ
Input Capacitor	10x10µF Ceramic	ESR=1.5mΩ

As a result of this loss analysis it becomes clear that the key to optimizing the efficiency of the proposed converter is reducing the resistive losses in the topology. One simple method to achieve this is to utilize a higher gate drive voltage. It was found experimentally that an 8V gate drive gives improved performance over a more standard 5V gate drive due to the reduced on-state resistance in the MOSFET's.

The input capacitor current waveform is shown in Figure 15. As M1 operates with 25% duty cycle, the input capacitor RMS current is given by:

$$I_{cRMS} = \sqrt{\left(\frac{3}{4}I_{out}\sqrt{0.25}\right)^2 + \left(\frac{1}{4}I_{out}\sqrt{0.75}\right)^2} = \frac{\sqrt{3}}{4}I_{out} \quad (18)$$

Thus the input capacitor should also utilize paralleled ceramic capacitors; large electrolytic capacitors are not suitable due to the large ESR.

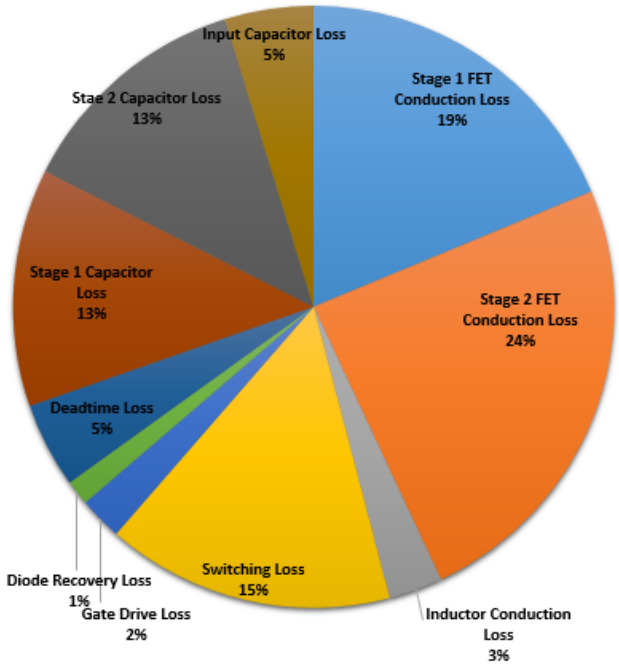

Fig. 14. Power Loss Analysis

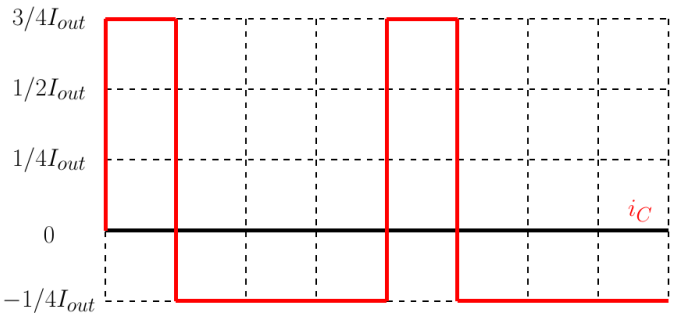

Fig. 15. Input Capacitor Current Waveforms

IV. Experimental Results

A prototype was constructed using the components outlined in Table 2. The experimental conditions are outlined in Table 3.

TABLE III. Loss Analysis Components

Experiment Parameters	
Switching Frequency	60kHz
Nominal Load Current	25A
Input Voltage	48V

Figure 16 shows the converter input voltage, the voltage of the two flying capacitors, and the output voltage. For the 48 volt input the first flying capacitor is charged to 1/2 V_{in}, or 24 volts, the second capacitor is charged to 1/4 V_{in}, or 12 volts, and the output voltage is also 12 volts.

Figure 17 shows the inductor current and voltage waveforms. As expected from the analysis conducted in Section 2, the inductor voltage waveform is equal to the sum of the capacitor voltage ripples. The effect of the deadtime on the inductor current is also shown.

Figure 18 shows the ripple voltage for both flying capacitors.

Figure 19 shows the voltage stress for MOSFET's M1 and M5. From this Figure it is clear that the voltage stress of the first MOSFET, M1, is reduced to approximately 1/2V_{in}, and the stress of the second MOSFET is reduced to approximately 1/4V_{in}. There is also very little ringing present in the V_{ds} waveforms for M1 and M5. It is important when designing the circuit that the inductance in the power circuit be made sufficiently small that the capacitor ESR and MOSFET on-resistance can damp it effectively. If the inductance is too large and the damping is poor, the voltage stress on the MOSFET's may increase, potentially damaging the devices.

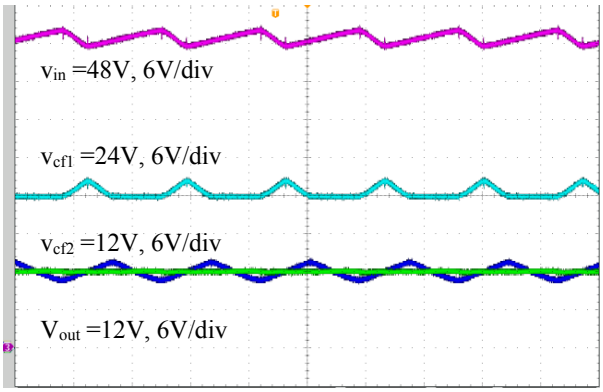

Fig. 16. Input Capacitor Current Waveforms, 25A load 60kHz

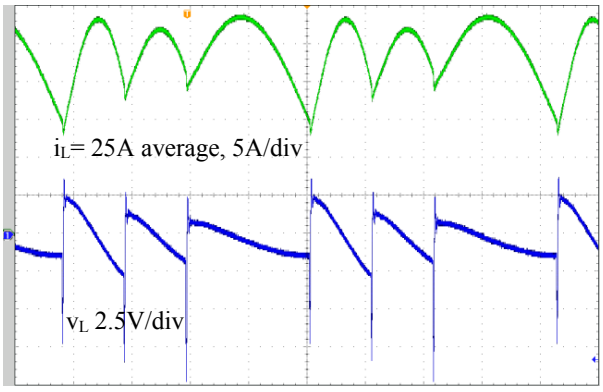

Fig. 17. Inductor Current and Voltage Waveforms, 25A load 60kHz

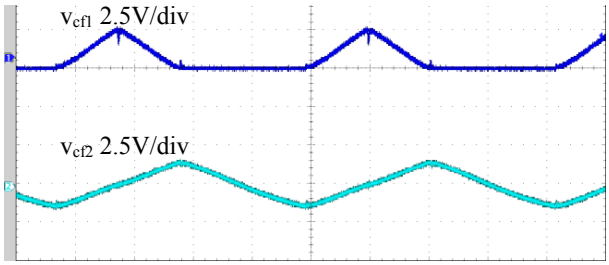

Fig. 18. Flying Capacitor Ripple Voltage Waveforms, 25A load 60kHz

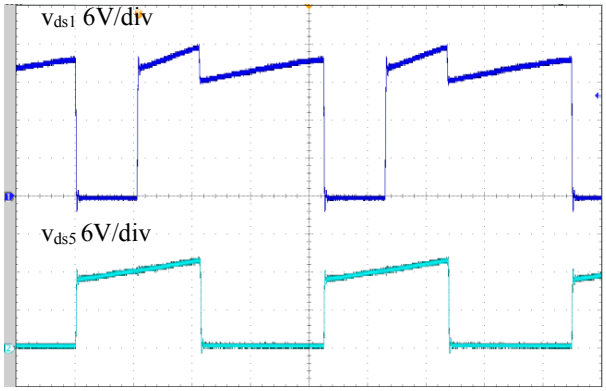

Fig. 19. Drain-to-Source Voltage Waveforms for M1 and M5, 25A load 60kHz

The load transient response is shown in Figures 20 and 21. The load is stepped from 1A to 20A with a slew rate of 10A/µsec (the maximum possible with the testing equipment available). There is very little overshoot and undershoot present in the output waveform. The reduction in output voltage is due partly to the resistive drop throughout the circuit, but it should be noted that the power supply is connected to the board through a long wire, and the voltage drop across this wire is not negligible. Thus part of the output voltage sag is due to the reduction in input voltage seen at the board's input terminals.

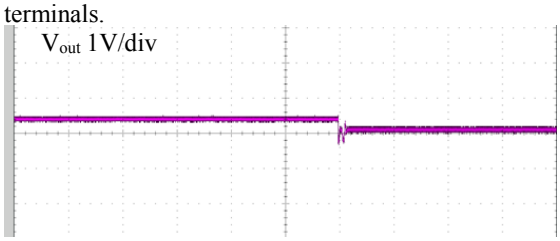

Fig. 20. Output Voltage Waveforms for Load Step of 1A to 20A

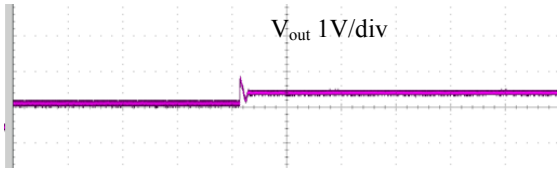

Fig. 21. Output Voltage Waveforms for Load Step of 20A to 1A

The measured efficiency of the experimental prototype, including the gate drive loss, is shown in Figure 22 in red. The peak efficiency is above 99.5% and the full load efficiency, at 35A (420W) output, is 98.1%. The efficiency without considering gate drive loss is also presented in blue.

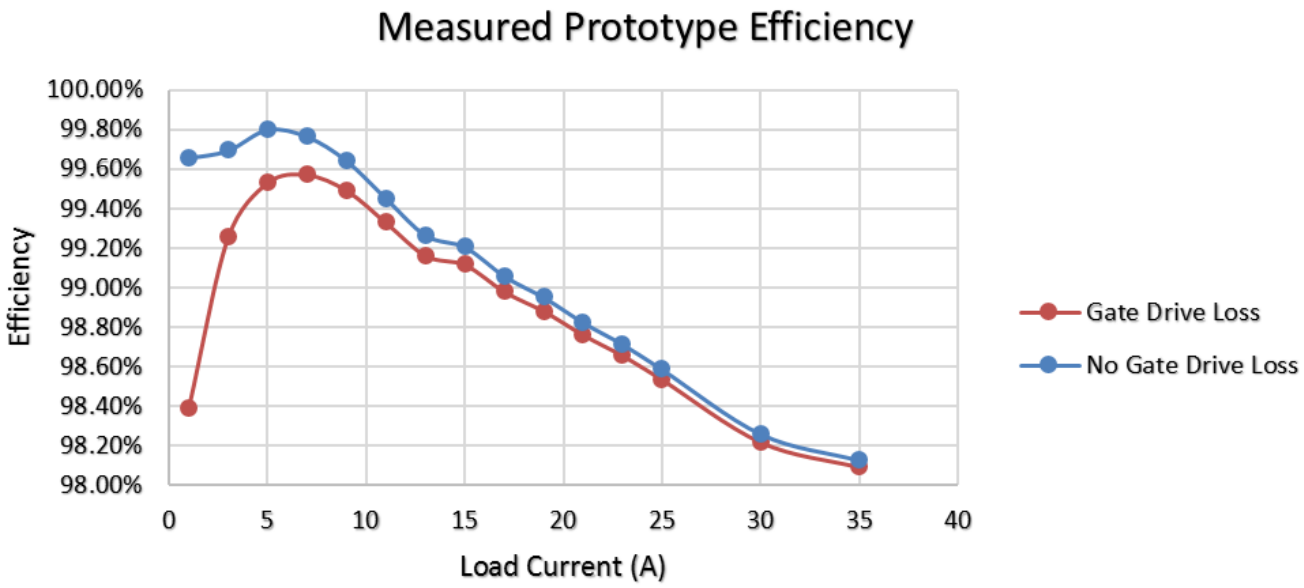

Fig. 22. Efficiency Measurements of the Prototype Converter

V. Conclusion

The topology presented in this paper addresses a key shift occurring in industry by achieving 48 volt to 12 volt conversion at an extremely high efficiency up to of 99.5%. Greater than 99% efficiency is maintained up to 17A (200W) output, and greater than 98.5% efficiency is maintained up to 25A (300W) output. The circuit also shows a very good transient response when dealing with large load step changes.

This topology has the potential to be a key enabler in the adoption of 48 volt server architecture by allowing for the benefits of higher voltage distribution to be maintained without losing these power savings in the step down to load voltages. Compared to a resonant converter topology, the design process is significantly simplified, and the converter is able to achieve superior performance in addition to this greatly simplified design process through the significant reduction in inductor loss enabled by the zero-inductor voltage operation.

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